

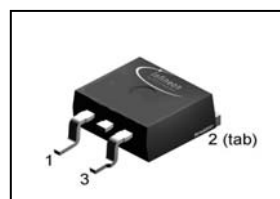
## OptiMOS<sup>®</sup> 2 Power-Transistor

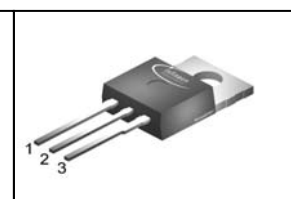
### Features

- Ideal for high-frequency dc/dc converters
- N-channel
- Logic level
- Excellent gate charge x  $R_{DS(on)}$  product (FOM)
- Very low on-resistance  $R_{DS(on)}$
- Superior thermal resistance
- 175 °C operating temperature
- dv/dt rated

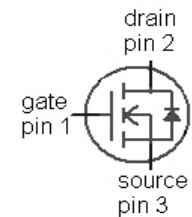
### Product Summary

$V_{DS}$	25	V
$R_{DS(on),max}$ (SMD version)	8.9	m $\Omega$
$I_D$	50	A

**P-TO263-3-2**

**P-TO262-3-1**

**P-TO220-3-1**


Type	Package	Ordering Code	Marking
IPB09N03LA	P-TO263-3-2	Q67042-S4151	09N03LA
IPI09N03LA	P-TO262-3-1	Q67042-S4152	09N03LA
IPP09N03LA	P-TO220-3-1	Q67042-S4153	09N03LA



**Maximum ratings, at  $T_j=25\text{ °C}$ , unless otherwise specified**

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	$I_D$	$T_C=25\text{ °C}^1)$	50	A
		$T_C=100\text{ °C}$	46	
Pulsed drain current	$I_{D,pulse}$	$T_C=25\text{ °C}^2)$	350	
Avalanche energy, single pulse	$E_{AS}$	$I_D=45\text{ A}, R_{GS}=25\ \Omega$	75	mJ
Reverse diode dv/dt	dv/dt	$I_D=50\text{ A}, V_{DS}=20\text{ V},$ $di/dt=200\text{ A}/\mu\text{s},$ $T_{j,max}=175\text{ °C}$	6	kV/ $\mu\text{s}$
Gate source voltage <sup>3)</sup>	$V_{GS}$		$\pm 20$	V
Power dissipation	$P_{tot}$	$T_C=25\text{ °C}$	63	W
Operating and storage temperature	$T_j, T_{stg}$		-55 ... 175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Thermal characteristics**

Thermal resistance, junction - case	$R_{thJC}$		-	-	2.4	K/W
SMD version, device on PCB	$R_{thJA}$	minimal footprint	-	-	62	
		6 cm <sup>2</sup> cooling area <sup>4)</sup>	-	-	40	

**Electrical characteristics, at  $T_j=25\text{ °C}$ , unless otherwise specified**
**Static characteristics**

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=1\text{ mA}$	25	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=20\text{ }\mu\text{A}$	1.2	1.6	2	
Zero gate voltage drain current	$I_{DSS}$	$V_{DS}=25\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ °C}$	-	0.1	1	$\mu\text{A}$
		$V_{DS}=25\text{ V}, V_{GS}=0\text{ V}, T_j=125\text{ °C}$	-	10	100	
Gate-source leakage current	$I_{GSS}$	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$	-	10	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=4.5\text{ V}, I_D=30\text{ A}$	-	12.4	15.5	m $\Omega$
		$V_{GS}=4.5\text{ V}, I_D=30\text{ A},$ SMD version	-	12.1	15.1	
		$V_{GS}=10\text{ V}, I_D=30\text{ A}$	-	7.7	9.2	
		$V_{GS}=10\text{ V}, I_D=30\text{ A},$ SMD version	-	7.4	8.9	
Gate resistance	$R_G$		-	1	-	$\Omega$
Transconductance	$g_{fs}$	$ V_{DS} >2 I_D R_{DS(on)max},$ $I_D=30\text{ A}$	21	42	-	S

<sup>1)</sup> Current is limited by bondwire; with an  $R_{thJC}=2.4\text{ K/W}$  the chip is able to carry 64 A.

<sup>2)</sup> See figure 3

<sup>3)</sup>  $T_{j,max}=150\text{ °C}$  and duty cycle  $D<0.25$  for  $V_{GS}<-5\text{ V}$

<sup>4)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70  $\mu\text{m}$  thick) copper area for drain connection. PCB is vertical in still air.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic characteristics**

Input capacitance	$C_{iss}$	$V_{GS}=0\text{ V}, V_{DS}=15\text{ V},$ $f=1\text{ MHz}$	-	1240	1649	pF
Output capacitance	$C_{oss}$		-	530	704	
Reverse transfer capacitance	$C_{rss}$		-	81	122	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=15\text{ V}, V_{GS}=10\text{ V},$ $I_D=25\text{ A}, R_G=2.7\ \Omega$	-	9	13	ns
Rise time	$t_r$		-	88	132	
Turn-off delay time	$t_{d(off)}$		-	22	33	
Fall time	$t_f$		-	4.2	6	

**Gate Charge Characteristics<sup>5)</sup>**

Gate to source charge	$Q_{gs}$	$V_{DD}=15\text{ V}, I_D=25\text{ A},$ $V_{GS}=0\text{ to }5\text{ V}$	-	4.4	5.8	nC
Gate charge at threshold	$Q_{g(th)}$		-	2.0	2.6	
Gate to drain charge	$Q_{gd}$		-	3.1	4.7	
Switching charge	$Q_{sw}$		-	5.5	7.9	
Gate charge total	$Q_g$		-	10	14	
Gate plateau voltage	$V_{plateau}$		-	3.5	-	V
Gate charge total, sync. FET	$Q_{g(sync)}$	$V_{DS}=0.1\text{ V},$ $V_{GS}=0\text{ to }5\text{ V}$	-	9	12	nC
Output charge	$Q_{oss}$	$V_{DD}=15\text{ V}, V_{GS}=0\text{ V}$	-	11	15	

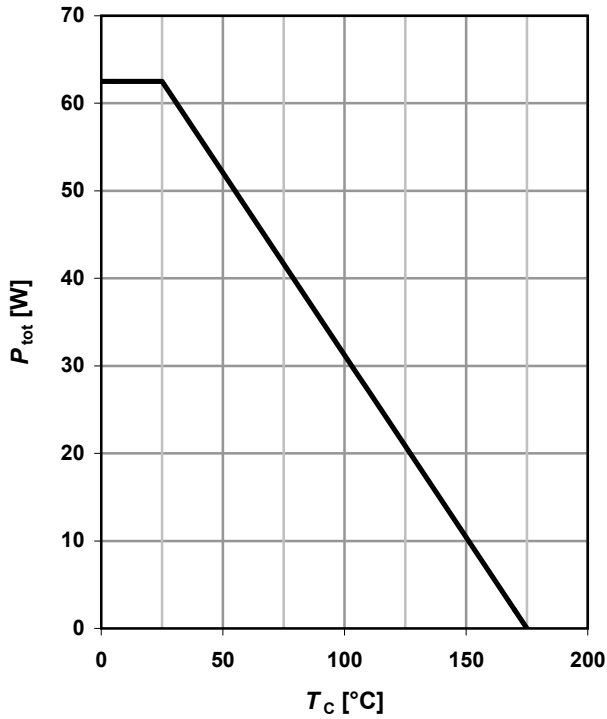
**Reverse Diode**

Diode continuous forward current	$I_S$	$T_C=25\text{ }^\circ\text{C}$	-	-	50	A
Diode pulse current	$I_{S,pulse}$		-	-	350	
Diode forward voltage	$V_{SD}$	$V_{GS}=0\text{ V}, I_F=50\text{ A},$ $T_j=25\text{ }^\circ\text{C}$	-	0.98	1.2	V
Reverse recovery charge	$Q_{rr}$	$V_R=15\text{ V}, I_F=I_S,$ $di_F/dt=400\text{ A}/\mu\text{s}$	-	-	10	nC

<sup>5)</sup> See figure 16 for gate charge parameter definition

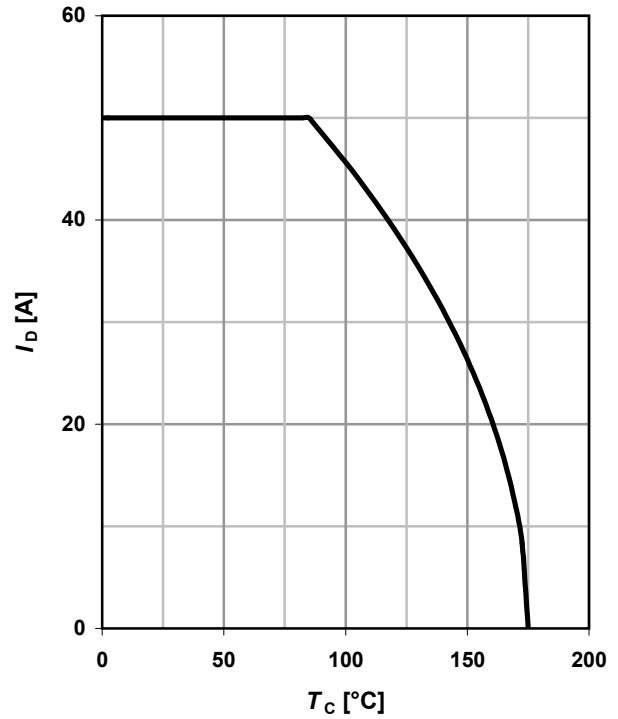
**1 Power dissipation**

$P_{tot}=f(T_C)$



**2 Drain current**

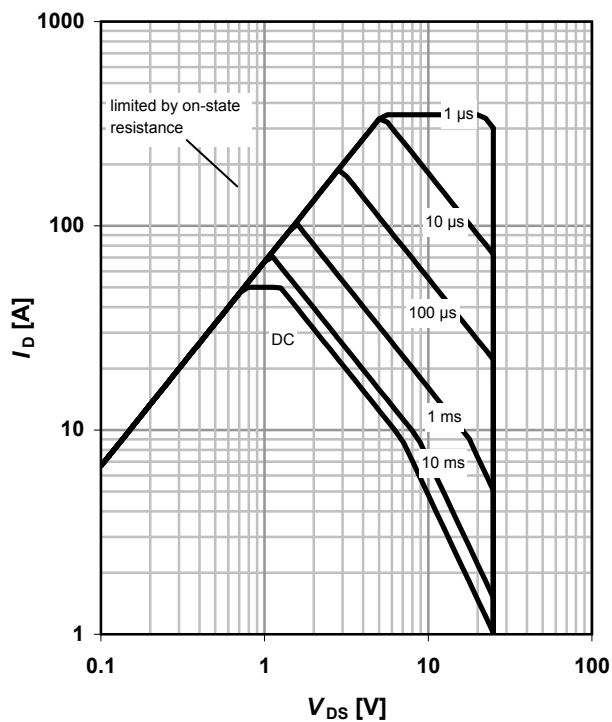
$I_D=f(T_C); V_{GS} \geq 10\text{ V}$



**3 Safe operation area**

$I_D=f(V_{DS}); T_C=25\text{ °C}; D=0$

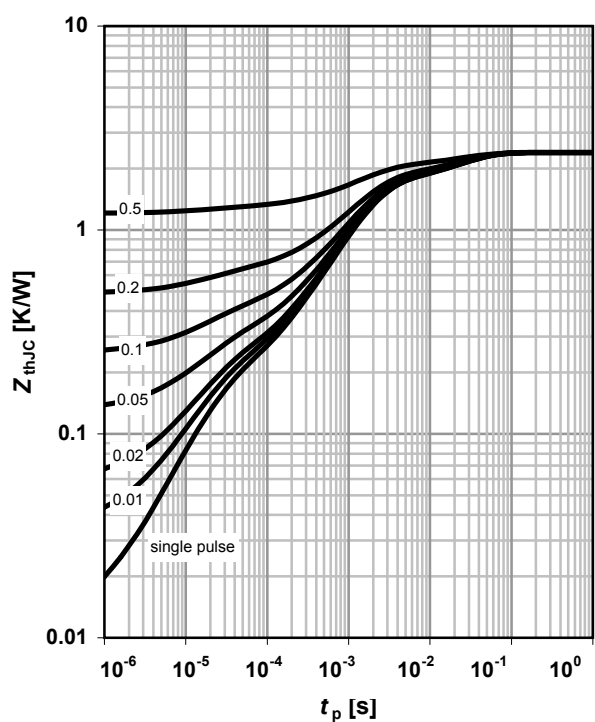
parameter:  $t_p$



**4 Max. transient thermal impedance**

$Z_{thJC}=f(t_p)$

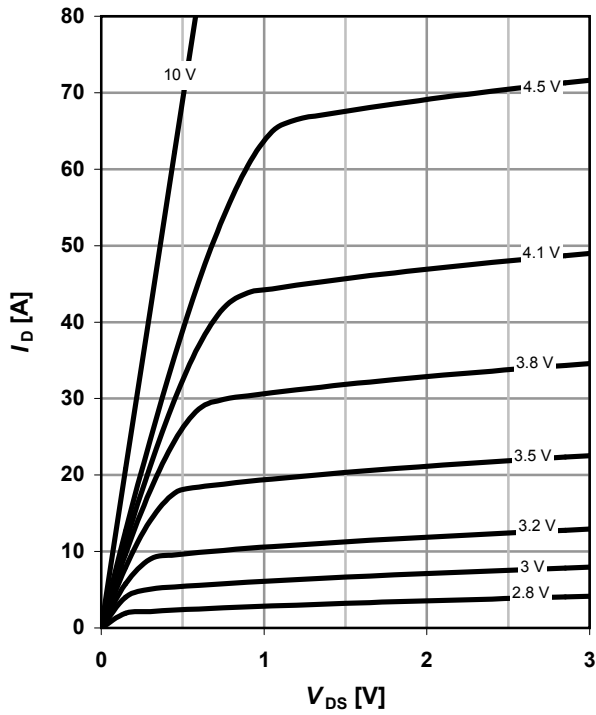
parameter:  $D=t_p/T$



**5 Typ. output characteristics**

$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$

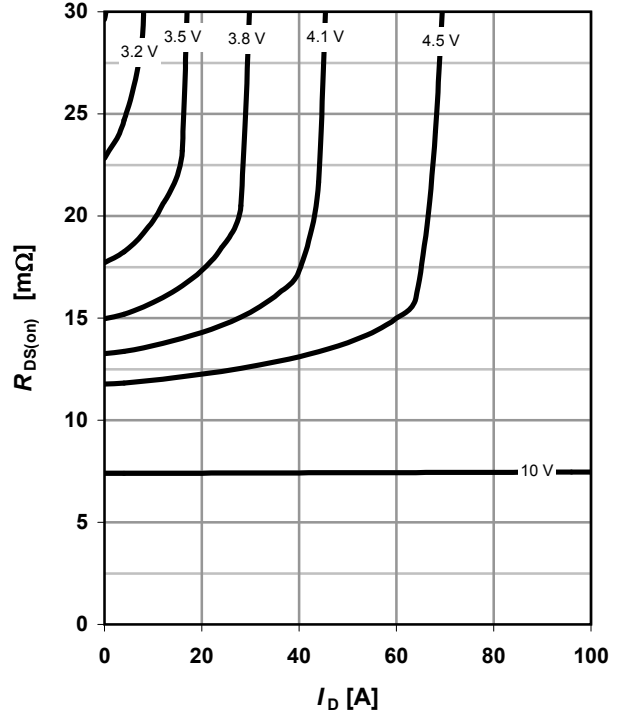
parameter:  $V_{GS}$



**6 Typ. drain-source on resistance**

$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

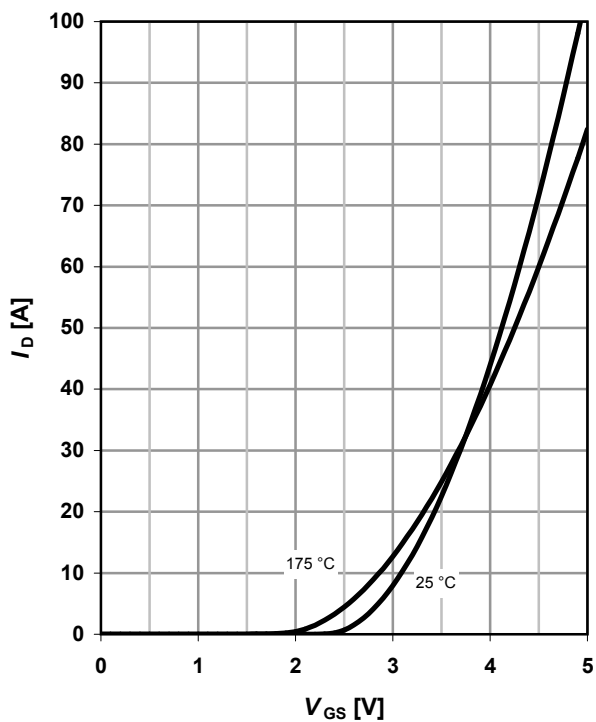
parameter:  $V_{GS}$



**7 Typ. transfer characteristics**

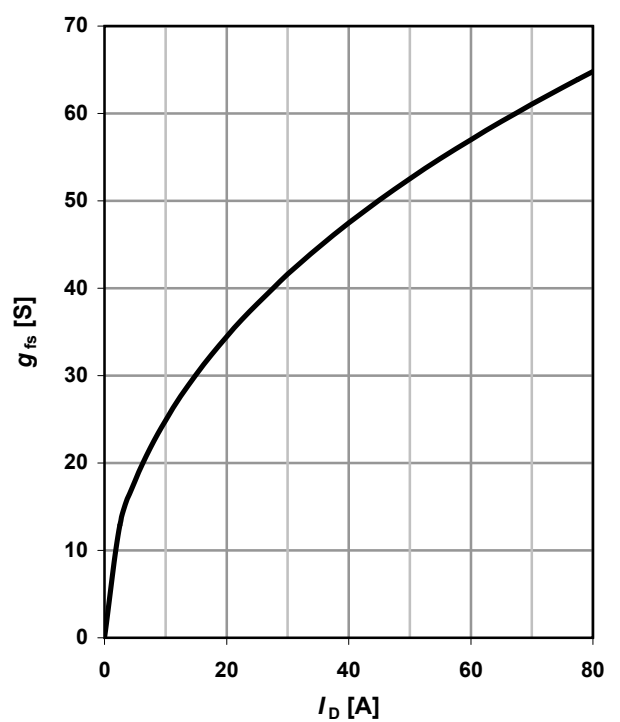
$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$

parameter:  $T_j$



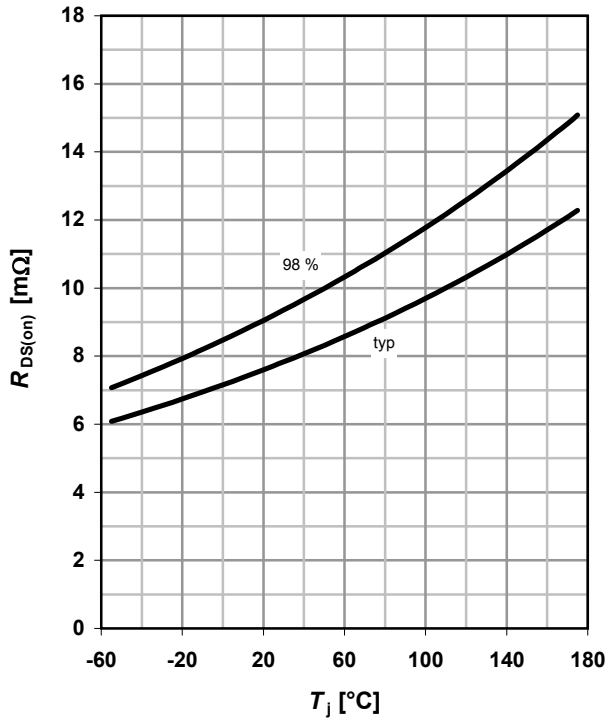
**8 Typ. forward transconductance**

$g_{fs} = f(I_D); T_j = 25\text{ }^\circ\text{C}$



**9 Drain-source on-state resistance**

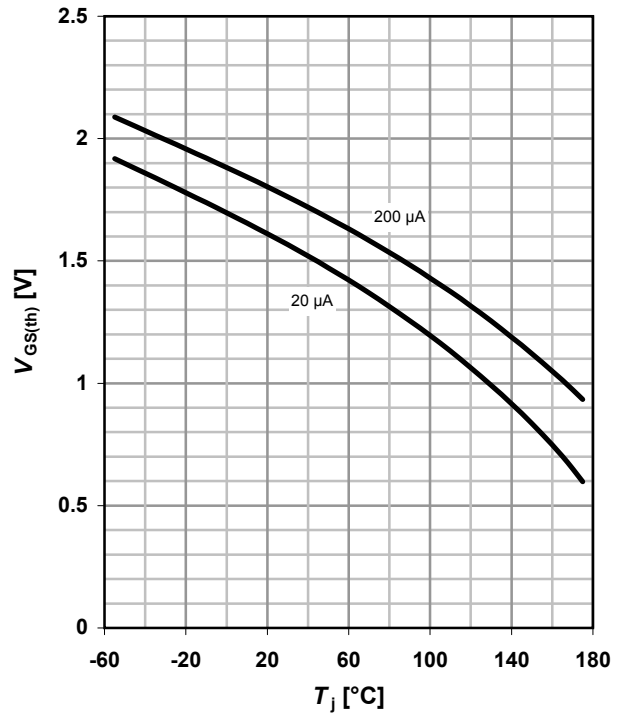
$R_{DS(on)} = f(T_j); I_D = 30 \text{ A}; V_{GS} = 10 \text{ V}$



**10 Typ. gate threshold voltage**

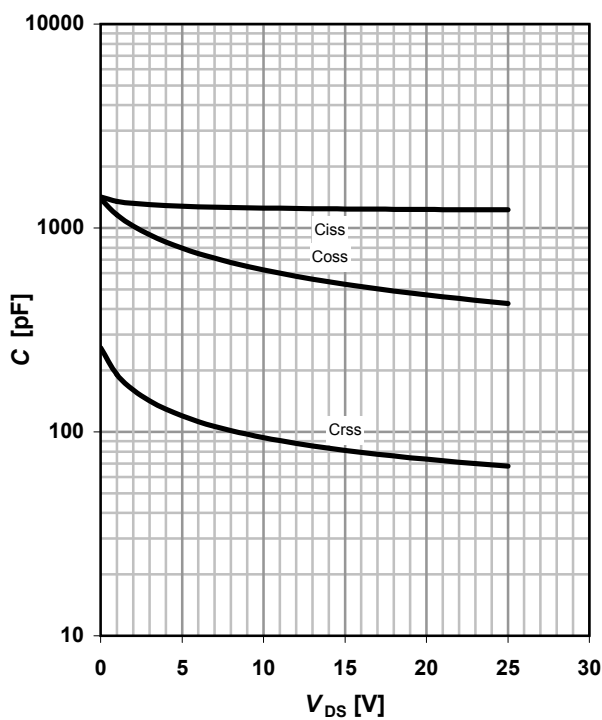
$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$

parameter:  $I_D$



**11 Typ. Capacitances**

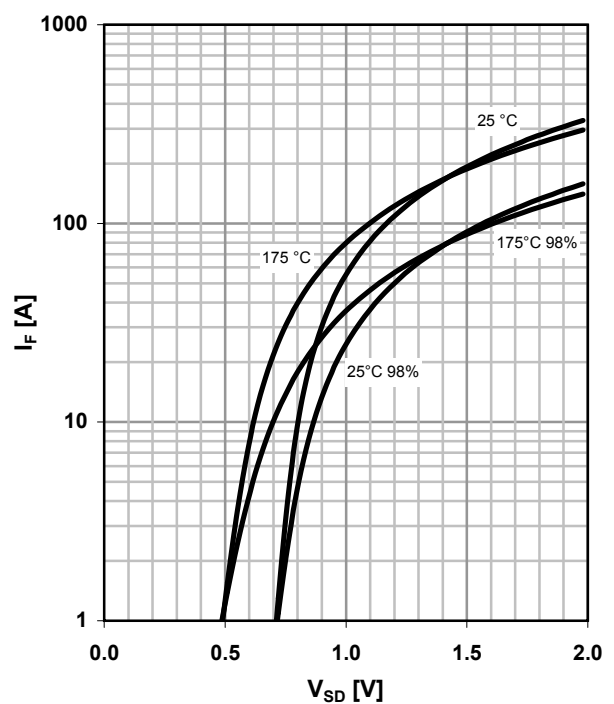
$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$



**12 Forward characteristics of reverse diode**

$I_F = f(V_{SD})$

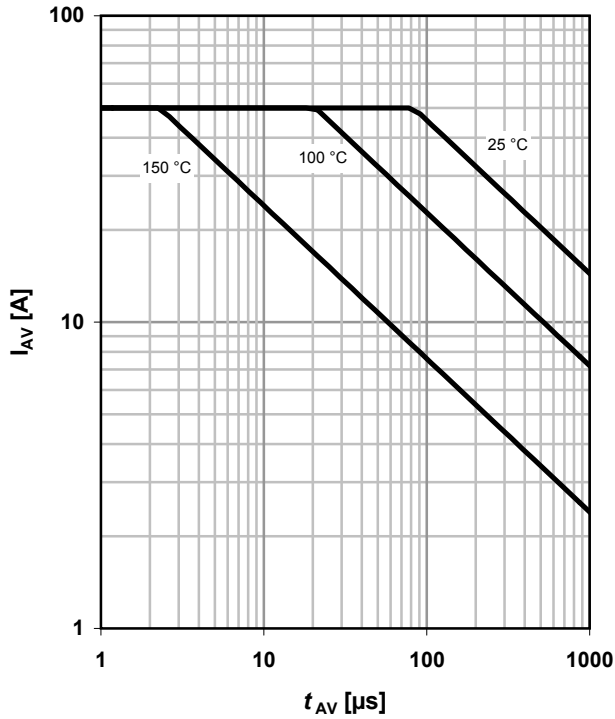
parameter:  $T_j$



**13 Avalanche characteristics**

$I_{AS}=f(t_{AV}); R_{GS}=25\ \Omega$

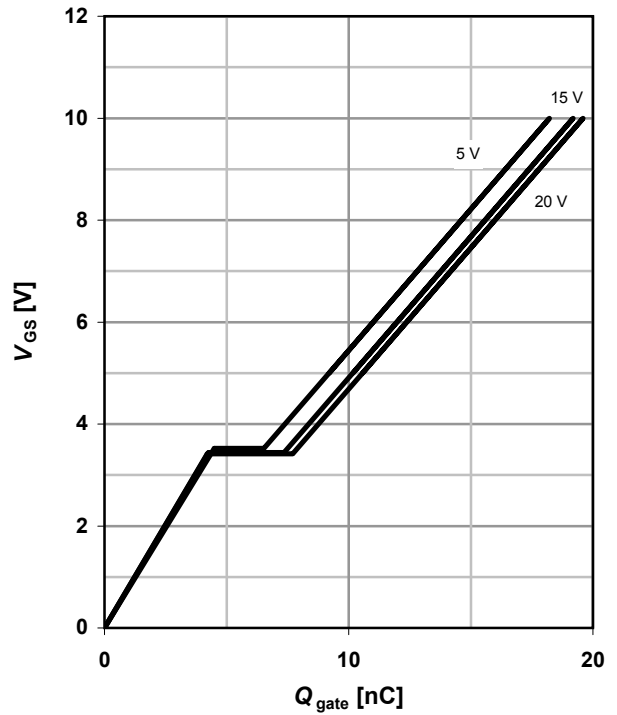
parameter:  $T_{j(\text{start})}$



**14 Typ. gate charge**

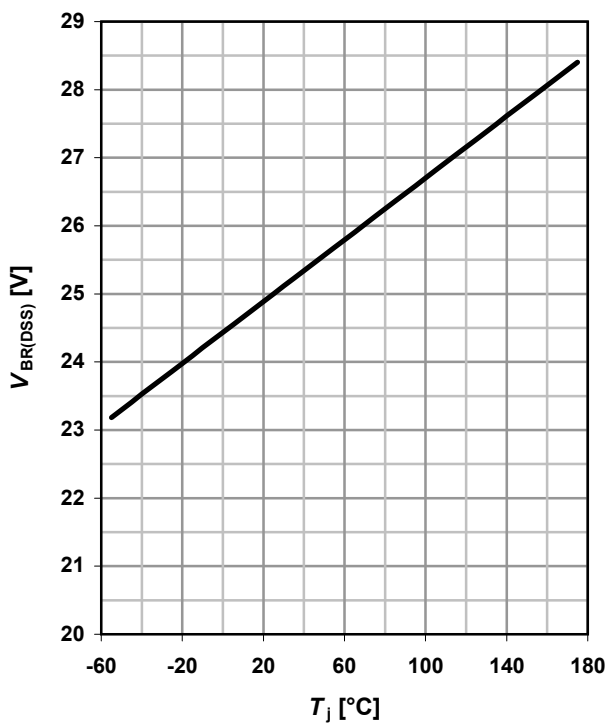
$V_{GS}=f(Q_{\text{gate}}); I_D=25\ \text{A pulsed}$

parameter:  $V_{DD}$

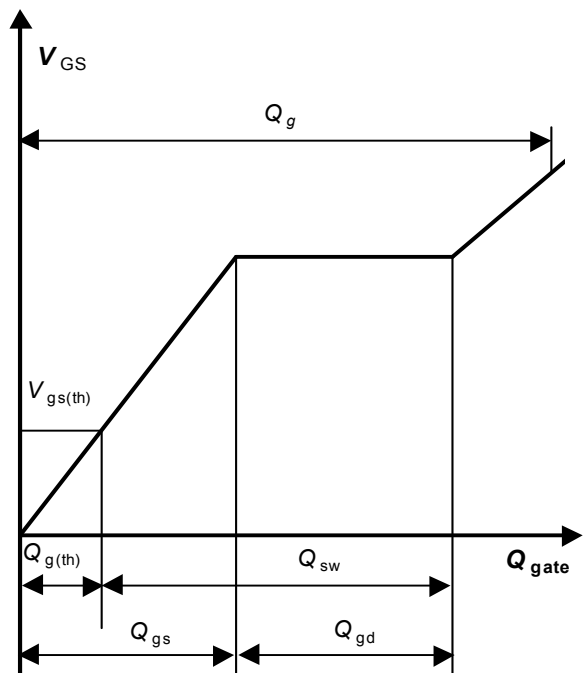


**15 Drain-source breakdown voltage**

$V_{BR(DSS)}=f(T_j); I_D=1\ \text{mA}$

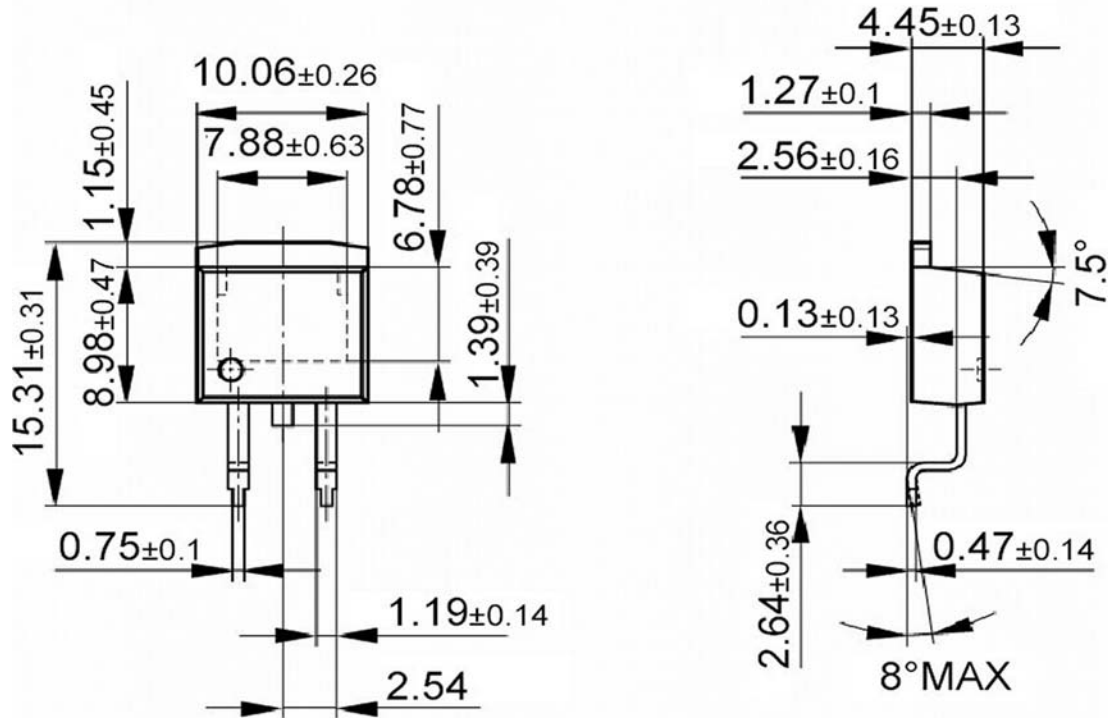


**16 Gate charge waveforms**

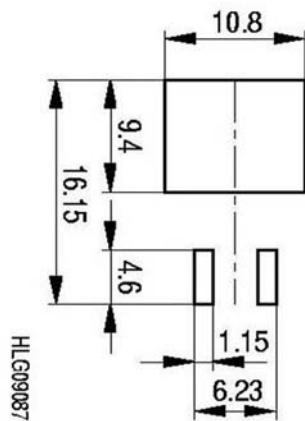


Package Outline

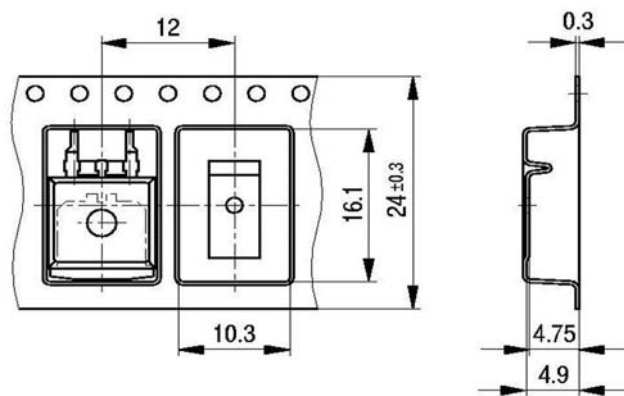
P-TO263-3-2: Outline



Footprint



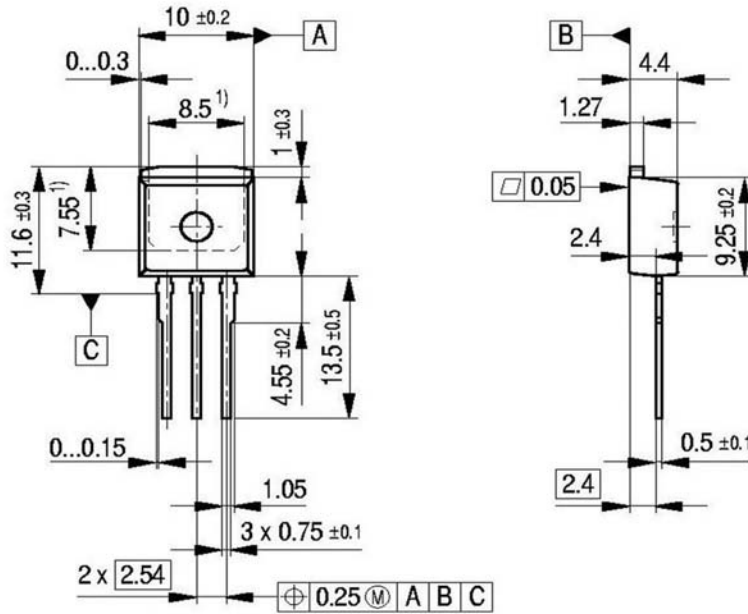
Packaging



Dimensions in mm

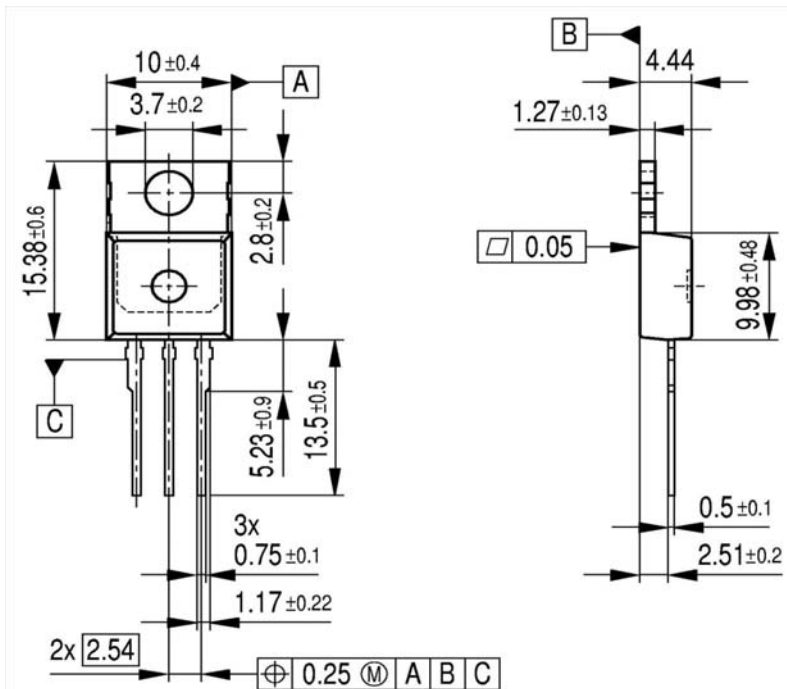


P-TO262-3-1: Outline



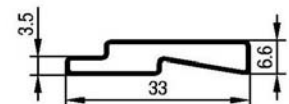
1) Typical  
 Metal surface min. X = 7.25, Y = 6.9  
 All metal surfaces tin plated, except area of cut.

P-TO220-3-1: Outline



All metal surfaces tin plated, except area of cut.  
 Metal surface min. x=7.25, y=12.3

Packaging



Dimensions in mm

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